UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/873,316	06/05/2001	Louis Jacobus Botha	RONI005/00US	5717

23446 7590 09/14/2006

MCANDREWS HELD & MALLOY, LTD
500 WEST MADISON STREET
SUITE 3400
CHICAGO, IL 60661

EXAMINER	
HO, CHUONG T	
ART UNIT	**PAPER NUMBER**
2616	

DATE MAILED: 09/14/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

38

Office Action Summary	Application No.	Applicant(s)
	09/873,316	BOTHA, LOUIS JACOBUS
	Examiner	**Art Unit**
	CHUONG T. HO	2616

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 June 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-6,9,11-15 and 17-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-6,9,11-15,17-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.

4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

5) ☐ Notice of Informal Patent Application

6) ☐ Other: _____.

1. The amendment filed 12/12/05 have been entered and made of record.

2. Applicant's arguments filed 06/28/06 have been fully considered but they are not persuasive.

Shiu discloses a memory buffer divided into logical partitions (col. 7, lines 1-5, a number of memory bands) representing radio frame block (col. 7, lines 1-5, radio frame) storing a single radio frame of data, each radio frame block being divided into two or more of the physical channel blocks (see col. 15, lines 33-35, For each radio frame interval, zero or more physical channels are received and processed, at step 612, to generate symbols that are then stored, at step 614, to permutated locations in a current memory bank associated with the radio frame), the single memory buffer comprising a separate single-ported memory device (see col. 7, lines 1-5, memory bank) for each radio frame block.

Shiu discloses the memory buffer being divided logically into radio frame blocks (see col. 7, lines 1-5, memory banks) and physical channel blocks (see col. 15, lines 33-35, physical channels), each radio frame block (see col. 7, lines 1-5, col. 15, lines 33-35, the memory banks) storing a single radio frame of data, each radio frame block being divided into two or more of the physical channel blocks (see col. 15, lines 33-35, For each radio frame interval, zero or more physical channels are received and processed, at step 612, to generate symbols that are then stored, at step 614, to permutated locations in a current memory bank associated with the radio frame).

Shiu discloses wherein said memory buffer comprises a dual-ported memory device (see col. 7, lines 1-5, memory buffer has a separate memory bank per radio frame) (see col. 15, lines 33-35, memory bank associated with the radio frame).

3. Claims 1, 3-6, 9, 11-15, 17-23 are pending.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1, 3-6, 9, 11-15, 17-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shiu et al. (U.S.Patent No. 6,624,767 B1) in view of Delvaux et al. (U.S.Patent No. 6,971,057 B1).

In the claim 1, see figure 2B, Shiu discloses referring back to FIG.2B, the processing from second de-interleaving 252 to first de-interleaving 264 can be efficiently achieved by properly managing buffer 512. Specially, the second de-interleaving 252 can be achieved by writing the symbols to buffer 512 in a second permutated order that is complementary to that performed for the second interleaving 238. The first de-interleaving 264 can be achieved by reading the symbols from buffer 512 in a first

permutated order that is complementary to that performed for the first interleaving 222 (see col. 13, lines 58-67); comprising:

- A single memory buffer divided into logical partitions (col. 7, lines 1-5, a number of memory bands) representing radio frame block (col. 7, lines 1-5, radio frame) storing a single radio frame of data, each radio frame block being divided into two or more of the physical channel blocks (see col. 15, lines 33-35, For each radio frame interval, zero or more physical channels are received and processed, at step 612, to generate symbols that are then stored, at step 614, to permutated locations in a current memory bank associated with the radio frame), the single memory buffer comprising a separate single-ported memory device (see col. 7, lines 1-5, memory bank) for each radio frame block.
- A memory buffer to store the data (see figure 2B, col. 13, lines 58-67, referring back to FIG.2B, the processing from second de-interleaving 252 to first de-interleaving 264 can be efficiently achieved by properly managing buffer 512. Specially, the second de-interleaving 252 can be achieved by writing the symbols to buffer 512 in a second permutated order that is complementary to that performed for the second interleaving 238. The first de-interleaving 264 can be achieved by reading the symbols from buffer 512 in a first permutated order that is complementary to that performed for the first interleaving 222; see col. 9, lines 22-25, second de-interleaving 252 can achieved at the receiver unit by writing the received symbols for each physical channel to the memory bank in a permutated order complementary to that used at the transmitter unit to achieve the second

interleaving, see col. 12, lines 27-30, first de-interleaving 264 can be achieved at the receiver unit by reading the received symbols for each traffic from memory banks in a permutated order complementary to that used at the transmitter unit to achieve the first interleaving;

- Unified means, coupled to memory buffer, for performing a first (264) and second (252) de-interleaving of the data stored in memory buffer, wherein means includes means for reading and writing the data to the memory buffer in connection with first (264) and second (252) de-interleaving (see figure 2B, col. 13, lines 58-67, referring back to FIG.2B, the processing from second de-interleaving 252 to first de-interleaving 264 can be efficiently achieved by properly managing buffer 512. Specially, the second de-interleaving 252 can be achieved by writing the symbols to buffer 512 in a second permutated order that is complementary to that performed for the second interleaving 238. The first de-interleaving 264 can be achieved by reading the symbols from buffer 512 in a first permutated order that is complementary to that performed for the first interleaving 222).

However, Shiu is silent to disclosing wherein said means applies a first portion of a second de-interleaving pattern as data is written to the single memory buffer, and wherein said means applies a second portion of second de-interleaving pattern as data is read from the single memory buffer.

Delvaux et al. discloses, (see figures 11a, 11b, col. 21, lines 13-17), the memory block 700 after a second de-interleave write and a second de-interleave read operation.

More specifically, bytes B0 through B10 have been written to their associated memory segments 710. It is significant to note that each byte of the second code word (i.e., bytes B0 through B10) appears in a memory segment identified by the initialization step (see col. 21, lines 14-16); comprising:

- See figure 11A, 11B, col. 21, lines 13-17, wherein said means applies a first portion (WRITE DATA: Bo, B1, B2, ..., B10) of a second de-interleaving pattern as data is written to the single memory buffer , and wherein said means applies a second portion (READ DATA: B0, X, X, X, X, A2, X, X, B1, X, X) of second de-interleaving pattern as data is read from the single memory buffer.

Both Shiu and Delvaux discloses de-interleaving radio frames. Delvaux et al. recognizes wherein said means applies a first portion of a second de-interleaving pattern as data is written to the single memory buffer , and wherein said means applies a second portion of second de-interleaving pattern as data is read from the single memory buffer. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the system of Shiu with the teaching of Delvaux to apply a first portion of a second de-interleaving pattern as data is written to the single memory buffer , and wherein said means applies a second portion of second de-interleaving pattern as data is read from the single memory buffer in order to improve the de-interleaving system.

5. In the claim 6, see figure 2B, Shiu discloses referring back to FIG.2B, the processing from second de-interleaving 252 to first de-interleaving 264 can be efficiently achieved by properly managing buffer 512. Specially, the second de-interleaving 252

can be achieved by writing the symbols to buffer 512 in a second permutated order that is complementary to that performed for the second interleaving 238. The first de-interleaving 264 can be achieved by reading the symbols from buffer 512 in a first permutated order that is complementary to that performed for the first interleaving 222 (see col. 13, lines 58-67); comprising:

- A demodulator (see col. 3, line 51, col. 13, line 27) coupled to the wireless link (see col. 3, lines 50-52); a decoding (see col. 5, lines 35-36)/ demultiplexing (see col. 5, lines 23-24) unit, coupled to demodulator (see col. 3, line 52, col. 13, lines 27);
- A memory buffer to store the data (see figure 2B, col. 13, lines 58-67, referring back to FIG.2B, the processing from second de-interleaving 252 to first de-interleaving 264 can be efficiently achieved by properly managing buffer 512. Specially, the second de-interleaving 252 can be achieved by writing the symbols to buffer 512 in a second permutated order that is complementary to that performed for the second interleaving 238. The first de-interleaving 264 can be achieved by reading the symbols from buffer 512 in a first permutated order that is complementary to that performed for the first interleaving 222; see col. 9, lines 22-25, second de-interleaving 252 can achieved at the receiver unit by writing the received symbols for each physical channel to the memory bank in a permutated order complementary to that used at the transmitter unit to achieve the second interleaving, see col. 12, lines 27-30, first de-interleaving 264 can be achieved at the receiver unit by reading the received symbols for each traffic from memory

banks in a permutated order complementary to that used at the transmitter unit to achieve the first interleaving;

- a memory buffer divided into logical partitions (col. 7, lines 1-5, a number of memory bands) representing radio frame block (col. 7, lines 1-5, radio frame) storing a single radio frame of data, each radio frame block being divided into two or more of the physical channel blocks (see col. 15, lines 33-35, For each radio frame interval, zero or more physical channels are received and processed, at step 612, to generate symbols that are then stored, at step 614, to permutated locations in a current memory bank associated with the radio frame), the single memory buffer comprising a separate single-ported memory device (see col. 7, lines 1-5, memory bank) for each radio frame block.
- Coupled to memory buffer, for performing a first (264) and second (252) de-interleaving of the data stored in memory buffer, wherein means includes means for reading and writing the data to the memory buffer in connection with first (264) and second (252) de-interleaving (see figure 2B, col. 13, lines 58-67, referring back to FIG.2B, the processing from second de-interleaving 252 to first de-interleaving 264 can be efficiently achieved by properly managing buffer 512. Specially, the second de-interleaving 252 can be achieved by writing the symbols to buffer 512 in a second permutated order that is complementary to that performed for the second interleaving 238. The first de-interleaving 264 can be achieved by reading the symbols from buffer 512 in a first permutated order that is complementary to that performed for the first interleaving 222); and a medium

access control layer coupled to decoding (see col. 13, lines 50-55) /demultiplexing (see col. 5, line 24, see col. 10, lines 57-58) unit;

- Wherein memory buffer store the data (see col. 6, lines 64-67);
- Wherein said means performs said second de-interleaving as the stored data is read from said memory buffer (see col. 6, lines 25-28);
- wherein said memory buffer comprises a dual-ported memory device (see col. 7, lines 1-5, memory buffer has a separate memory bank per radio frame) (see col. 15, lines 33-35, memory bank associated with the radio frame).

However, Shiu is silent to disclosing wherein said means applies a first portion of a second de-interleaving pattern as data is written to the single memory buffer, and wherein said means applies a second portion of second de-interleaving pattern as data is read from the single memory buffer.

Delvaux et al. discloses, (see figures 11a, 11b, col. 21, lines 13-17), the memory block 700 after a second de-interleave write and a second de-interleave read operation. More specifically, bytes B0 through B10 have been written to their associated memory segments 710. It is significant to note that each byte of the second code word (i.e., bytes B0 through B10) appears in a memory segment identified by the initialization step (see col. 21, lines 14-16); comprising:

- See figure 11A, 11B, col. 21, lines 13-17, wherein said means applies a first portion (WRITE DATA: Bo, B1, B2, ..., B10) of a second de-interleaving pattern as data is written to the single memory buffer , and wherein said means applies a

second portion (READ DATA: B0, X, X, X, X, A2, X, X, B1, X, X) of second de-interleaving pattern as data is read from the single memory buffer.

Both Shiu and Delvaux discloses de-interleaving radio frames. Delvaux et al. recognizes wherein said means applies a first portion of a second de-interleaving pattern as data is written to the single memory buffer , and wherein said means applies a second portion of second de-interleaving pattern as data is read from the single memory buffer. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the system of Shiu with the teaching of Delvaux to apply a first portion of a second de-interleaving pattern as data is written to the single memory buffer , and wherein said means applies a second portion of second de-interleaving pattern as data is read from the single memory buffer in order to improve the de-interleaving system.

6. In the claim 9, see figure 2B, Shiu discloses referring back to FIG.2B, the processing from second de-interleaving 252 to first de-interleaving 264 can be efficiently achieved by properly managing buffer 512. Specially, the second de-interleaving 252 can be achieved by writing the symbols to buffer 512 in a second permutated order that is complementary to that performed for the second interleaving 238. The first de-interleaving 264 can be achieved by reading the symbols from buffer 512 in a first permutated order that is complementary to that performed for the first interleaving 222 (see col. 13, lines 58-67); comprising:

- A memory buffer to store the data (see figure 2B, col. 13, lines 58-67, referring back to FIG.2B, the processing from second de-interleaving 252 to first de-

interleaving 264 can be efficiently achieved by properly managing buffer 512. Specially, the second de-interleaving 252 can be achieved by writing the symbols to buffer 512 in a second permutated order that is complementary to that performed for the second interleaving 238. The first de-interleaving 264 can be achieved by reading the symbols from buffer 512 in a first permutated order that is complementary to that performed for the first interleaving 222; see col. 9, lines 22-25, second de-interleaving 252 can achieved at the receiver unit by writing the received symbols for each physical channel to the memory bank in a permutated order complementary to that used at the transmitter unit to achieve the second interleaving, see col. 12, lines 27-30, first de-interleaving 264 can be achieved at the receiver unit by reading the received symbols for each traffic from memory banks in a permutated order complementary to that used at the transmitter unit to achieve the first interleaving;

- a memory buffer divided into logical partitions (col. 7, lines 1-5, a number of memory bands) representing radio frame block (col. 7, lines 1-5, radio frame) storing a single radio frame of data, each radio frame block being divided into two or more of the physical channel blocks (see col. 15, lines 33-35, For each radio <u>frame interval, zero or more physical channels</u> are received and processed, at step 612, to generate symbols that are then stored, at step 614, to permutated locations in a current memory bank associated with the radio frame), the single memory buffer comprising a separate single-ported memory device (see col. 7, lines 1-5, memory bank) for each radio frame block.

- Coupled to memory buffer, for performing a first (264) and second (252) de-interleaving of the data stored in memory buffer, wherein means includes means for reading and writing the data to the memory buffer in connection with first (264) and second (252) de-interleaving (see figure 2B, col. 13, lines 58-67, referring back to FIG.2B, the processing from second de-interleaving 252 to first de-interleaving 264 can be efficiently achieved by properly managing buffer 512. Specially, the second de-interleaving 252 can be achieved by writing the symbols to buffer 512 in a second permutated order that is complementary to that performed for the second interleaving 238. The first de-interleaving 264 can be achieved by reading the symbols from buffer 512 in a first permutated order that is complementary to that performed for the first interleaving 222);
- Wherein the memory buffer comprises multiple memory device (see col. 7, lines 1-5, memory banks) in which logical divisions do not correspond to physical divisions between the devices.

However, Shiu is silent to disclosing wherein said means applies a first portion of a second de-interleaving pattern as data is written to the single memory buffer, and wherein said means applies a second portion of second de-interleaving pattern as data is read from the single memory buffer.

Delvaux et al. discloses, (see figures 11a, 11b, col. 21, lines 13-17), the memory block 700 after a second de-interleave write and a second de-interleave read operation. More specifically, bytes B0 through B10 have been written to their associated memory segments 710. It is significant to note that each byte of the second code word (i.e.,

bytes B0 through B10) appears in a memory segment identified by the initialization step (see col. 21, lines 14-16); comprising:

- See figure 11A, 11B, col. 21, lines 13-17, wherein said means applies a first portion (WRITE DATA: Bo, B1, B2, ..., B10) of a second de-interleaving pattern as data is written to the single memory buffer , and wherein said means applies a second portion (READ DATA: B0, X, X, X; X, A2, X, X, B1, X, X) of second de-interleaving pattern as data is read from the single memory buffer.

Both Shiu and Delvaux discloses de-interleaving radio frames. Delvaux et al. recognizes wherein said means applies a first portion of a second de-interleaving pattern as data is written to the single memory buffer , and wherein said means applies a second portion of second de-interleaving pattern as data is read from the single memory buffer. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the system of Shiu with the teaching of Delvaux to apply a first portion of a second de-interleaving pattern as data is written to the single memory buffer , and wherein said means applies a second portion of second de-interleaving pattern as data is read from the single memory buffer in order to improve the de-interleaving system.

7. In the claim 11, see figure 2B, Shiu discloses referring back to FIG.2B, the processing from second de-interleaving 252 to first de-interleaving 264 can be efficiently achieved by properly managing buffer 512. Specially, the second de-interleaving 252 can be achieved by writing the symbols to buffer 512 in a second permutated order that is complementary to that performed for the second interleaving 238. The first de-

interleaving 264 can be achieved by reading the symbols from buffer 512 in a first permutated order that is complementary to that performed for the first interleaving 222 (see col. 13, lines 58-67); comprising:

- Logical divided a memory buffer into radio frame blocks and physical channel blocks, each radio frame block storing a single radio frame of data, each radio frame block being divide into two or more of the physical channel blocks (col. 7, lines 1-5, a number of memory bands) (col. 7, lines 1-5, radio frame) (see col. 15, lines 33-35, For each radio frame interval, zero or more physical channels are received and processed, at step 612, to generate symbols that are then stored, at step 614, to permutated locations in a current memory bank associated with the radio frame), the single memory buffer comprising a separate single-ported memory device (see col. 7, lines 1-5, memory bank) for each radio frame block.
- A memory buffer to store the data (see figure 2B, col. 13, lines 58-67, referring back to FIG.2B, the processing from second de-interleaving 252 to first de-interleaving 264 can be efficiently achieved by properly managing buffer 512. Specially, the second de-interleaving 252 can be achieved by writing the symbols to buffer 512 in a second permutated order that is complementary to that performed for the second interleaving 238. The first de-interleaving 264 can be achieved by reading the symbols from buffer 512 in a first permutated order that is complementary to that performed for the first interleaving 222; see col. 9, lines 22-25, second de-interleaving 252 can achieved at the receiver unit by writing the received symbols for each physical channel to the memory bank in a permutated

order complementary to that used at the transmitter unit to achieve the second interleaving, see col. 12, lines 27-30, first de-interleaving 264 can be achieved at the receiver unit by reading the received symbols for each traffic from memory banks in a permutated order complementary to that used at the transmitter unit to achieve the first interleaving;

- Coupled to memory buffer, for performing a first (264) and second (252) de-interleaving of the data stored in memory buffer, wherein means includes means for reading and writing the data to the memory buffer in connection with first (264) and second (252) de-interleaving (see figure 2B, col. 13, lines 58-67, referring back to FIG.2B, the processing from second de-interleaving 252 to first de-interleaving 264 can be efficiently achieved by properly managing buffer 512. Specially, the second de-interleaving 252 can be achieved by writing the symbols to buffer 512 in a second permutated order that is complementary to that performed for the second interleaving 238. The first de-interleaving 264 can be achieved by reading the symbols from buffer 512 in a first permutated order that is complementary to that performed for the first interleaving 222);
- Performing a first de-interleaving as data is read from memory buffer (see col. 6, lines 33-35, the first de-interleaving 264, the symbols for each transport channel can be written to sequential locations in another memory and **read out** in a permutated order);

- The data being written into a rectangular matrix (see col. 6, lines 11-12, the first interleaving stage 222, the input bits are written row-by-row to an R row by C column rectangular matrix starting from the first column of the first row.)

However, Shiu is silent to disclosing wherein said means applies a first portion of a second de-interleaving pattern as data is written to the single memory buffer, and wherein said means applies a second portion of second de-interleaving pattern as data is read from the single memory buffer.

Delvaux et al. discloses, (see figures 11a, 11b, col. 21, lines 13-17), the memory block 700 after a second de-interleave write and a second de-interleave read operation. More specifically, bytes B0 through B10 have been written to their associated memory segments 710. It is significant to note that each byte of the second code word (i.e., bytes B0 through B10) appears in a memory segment identified by the initialization step (see col. 21, lines 14-16); comprising:

- See figure 11A, 11B, col. 21, lines 13-17, wherein said means applies a first portion (WRITE DATA: Bo, B1, B2, ..., B10) of a second de-interleaving pattern as data is written to the single memory buffer, and wherein said means applies a second portion (READ DATA: B0, X, X, X, X, A2, X, X, B1, X, X) of second de-interleaving pattern as data is read from the single memory buffer.

Both Shiu and Delvaux discloses de-interleaving radio frames. Delvaux et al. recognizes wherein said means applies a first portion of a second de-interleaving pattern as data is written to the single memory buffer , and wherein said means applies a second portion of second de-interleaving pattern as data is read from the single

memory buffer. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the system of Shiu with the teaching of Delvaux to apply a first portion of a second de-interleaving pattern as data is written to the single memory buffer , and wherein said means applies a second portion of second de-interleaving pattern as data is read from the single memory buffer in order to improve the de-interleaving system.

8. In the claim 13, see figure 2B, Shiu discloses referring back to FIG.2B, the processing from second de-interleaving 252 to first de-interleaving 264 can be efficiently achieved by properly managing buffer 512. Specially, the second de-interleaving 252 can be achieved by writing the symbols to buffer 512 in a second permutated order that is complementary to that performed for the second interleaving 238. The first de-interleaving 264 can be achieved by reading the symbols from buffer 512 in a first permutated order that is complementary to that performed for the first interleaving 222 (see col. 13, lines 58-67); comprising:

- A demodulator (see col. 3, line 51, col. 13, line 27) coupled to the wireless link (see col. 3, lines 50-52);
- A memory buffer to store the data (see figure 2B, col. 13, lines 58-67, referring back to FIG.2B, the processing from second de-interleaving 252 to first de-interleaving 264 can be efficiently achieved by properly managing buffer 512. Specially, the second de-interleaving 252 can be achieved by writing the symbols to buffer 512 in a second permutated order that is complementary to that performed for the second interleaving 238. The first de-interleaving 264 can be

achieved by reading the symbols from buffer 512 in a first permutated order that is complementary to that performed for the first interleaving 222; see col. 9, lines 22-25, second de-interleaving 252 can achieved at the receiver unit by writing the received symbols for each physical channel to the memory bank in a permutated order complementary to that used at the transmitter unit to achieve the second interleaving, see col. 12, lines 27-30, first de-interleaving 264 can be achieved at the receiver unit by reading the received symbols for each traffic from memory banks in a permutated order complementary to that used at the transmitter unit to achieve the first interleaving;

- a memory buffer divided into logical partitions (col. 7, lines 1-5, a number of memory bands) representing radio frame block (col. 7, lines 1-5, radio frame) storing a single radio frame of data, each radio frame block being divided into two or more of the physical channel blocks (see col. 15, lines 33-35, For each radio <u>frame interval, zero or more physical channels</u> are received and processed, at step 612, to generate symbols that are then stored, at step 614, to permutated locations in a current memory bank associated with the radio frame), the single memory buffer comprising a separate single-ported memory device (see col. 7, lines 1-5, memory bank) for each radio frame block.
- Coupled to memory buffer, for performing a first (264) and second (252) de-interleaving of the data stored in memory buffer, wherein means includes means for reading and writing the data to the memory buffer in connection with first (264) and second (252) de-interleaving (see figure 2B, col. 13, lines 58-67,

referring back to FIG.2B, the processing from second de-interleaving 252 to first de-interleaving 264 can be efficiently achieved by properly managing buffer 512. Specially, the second de-interleaving 252 can be achieved by writing the symbols to buffer 512 in a second permutated order that is complementary to that performed for the second interleaving 238. The first de-interleaving 264 can be achieved by reading the symbols from buffer 512 in a first permutated order that is complementary to that performed for the first interleaving 222); decoding (see col. 13, lines 50-55) the output data stream;

- Storing the demodulated data in a memory buffer (see col. 6, lines 64-67);
- Reading said data from said memory buffer according to a second de-interleaving pattern (see col. 6, lines 25-28);
- Reading said data from said memory buffer according to a first de-interleaving pattern, forming an output data stream (see col. 6, lines 33-35);
- Decoding output data stream (see col. 5, lines 35-36).

However, Shiu is silent to disclosing wherein said means applies a first portion of a second de-interleaving pattern as data is written to the single memory buffer, and wherein said means applies a second portion of second de-interleaving pattern as data is read from the single memory buffer.

Delvaux et al. discloses, (see figures 11a, 11b, col. 21, lines 13-17), the memory block 700 after a second de-interleave write and a second de-interleave read operation. More specifically, bytes B0 through B10 have been written to their associated memory segments 710. It is significant to note that each byte of the second code word (i.e.,

bytes B0 through B10) appears in a memory segment identified by the initialization step (see col. 21, lines 14-16); comprising:

- See figure 11A, 11B, col. 21, lines 13-17, writing (WRITE DATA: Bo, B1, B2, ..., B10) said data to said memory buffer to effectively perform a first portion of a second de-interleaving pattern; reading portion (READ DATA: B0, X, X, X, X, A2, X, X, B1, X, X) said data from said memory buffer to form an output data stream; wherein said reading effectively performs a second portion of a second de-interleaving pattern and a first de-interleaving pattern (see figure 11A, 11B, col. 21, lines 13-17, a first de-interleaving read operation......a second de-interleave read operation).

Both Shiu and Delvaux discloses de-interleaving radio frames. Delvaux et al. recognizes wherein said means applies a first portion of a second de-interleaving pattern as data is written to the single memory buffer , and wherein said means applies a second portion of second de-interleaving pattern as data is read from the single memory buffer. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the system of Shiu with the teaching of Delvaux to apply a first portion of a second de-interleaving pattern as data is written to the single memory buffer , and wherein said means applies a second portion of second de-interleaving pattern as data is read from the single memory buffer in order to improve the de-interleaving system.

9. In the claim 15, see figure 2B, Shiu discloses referring back to FIG.2B, the processing from second de-interleaving 252 to first de-interleaving 264 can be efficiently

achieved by properly managing buffer 512. Specially, the second de-interleaving 252 can be achieved by writing the symbols to buffer 512 in a second permutated order that is complementary to that performed for the second interleaving 238. The first de-interleaving 264 can be achieved by reading the symbols from buffer 512 in a first permutated order that is complementary to that performed for the first interleaving 222 (see col. 13, lines 58-67); comprising:

- A demodulator (see col. 3, line 51, col. 13, line 27) configured to demodulate the data;
- A memory buffer to store the data (see figure 2B, col. 13, lines 58-67, referring back to FIG.2B, the processing from second de-interleaving 252 to first de-interleaving 264 can be efficiently achieved by properly managing buffer 512. Specially, the second de-interleaving 252 can be achieved by writing the symbols to buffer 512 in a second permutated order that is complementary to that performed for the second interleaving 238. The first de-interleaving 264 can be achieved by reading the symbols from buffer 512 in a first permutated order that is complementary to that performed for the first interleaving 222; see col. 9, lines 22-25, second de-interleaving 252 can achieved at the receiver unit by writing the received symbols for each physical channel to the memory bank in a permutated order complementary to that used at the transmitter unit to achieve the second interleaving, see col. 12, lines 27-30, first de-interleaving 264 can be achieved at the receiver unit by reading the received symbols for each traffic from memory

banks in a permutated order complementary to that used at the transmitter unit to achieve the first interleaving);

- a memory buffer divided into logical partitions (col. 7, lines 1-5, a number of memory bands) representing radio frame block (col. 7, lines 1-5, radio frame) storing a single radio frame of data, each radio frame block being divided into two or more of the physical channel blocks (see col. 15, lines 33-35, For each radio frame interval, zero or more physical channels are received and processed, at step 612, to generate symbols that are then stored, at step 614, to permutated locations in a current memory bank associated with the radio frame), the single memory buffer comprising a separate single-ported memory device (see col. 7, lines 1-5, memory bank) for each radio frame block.
- Coupled to memory buffer, for performing a first (264) and second (252) de-interleaving of the data stored in memory buffer, wherein means includes means for reading and writing the data to the memory buffer in connection with first (264) and second (252) de-interleaving (see figure 2B, col. 13, lines 58-67, referring back to FIG.2B, the processing from second de-interleaving 252 to first de-interleaving 264 can be efficiently achieved by properly managing buffer 512. Specially, the second de-interleaving 252 can be achieved by writing the symbols to buffer 512 in a second permutated order that is complementary to that performed for the second interleaving 238. The first de-interleaving 264 can be achieved by reading the symbols from buffer 512 in a first permutated order that is complementary to that performed for the first interleaving 222);

- Wherein said memory buffer stores the data (see col. 6, lines 64-67);
- Wherein said means performs said second de-interleaving as the stored data is read from said memory buffer (see col. 6, lines 25-28).

However, Shiu is silent to disclosing wherein said means applies a first portion of a second de-interleaving pattern as data is written to the single memory buffer, and wherein said means applies a second portion of second de-interleaving pattern as data is read from the single memory buffer.

Delvaux et al. discloses, (see figures 11a, 11b, col. 21, lines 13-17), the memory block 700 after a second de-interleave write and a second de-interleave read operation. More specifically, bytes B0 through B10 have been written to their associated memory segments 710. It is significant to note that each byte of the second code word (i.e., bytes B0 through B10) appears in a memory segment identified by the initialization step (see col. 21, lines 14-16); comprising:

- See figure 11A, 11B, col. 21, lines 13-17, wherein said means performs a first portion of said second de-interleaving as the data is written into the memory buffer and said means performs a second of said second de-interleaving and said first de-interleaving as the written data is read from said memory buffer (see figure 11A, 11B, col. 21, lines 13-17, a first de-interleaving read operation......a second de-interleave read operation).

Both Shiu and Delvaux discloses de-interleaving radio frames. Delvaux et al. recognizes wherein said means applies a first portion of a second de-interleaving pattern as data is written to the single memory buffer , and wherein said means applies

a second portion of second de-interleaving pattern as data is read from the single memory buffer. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the system of Shiu with the teaching of Delvaux to apply a first portion of a second de-interleaving pattern as data is written to the single memory buffer , and wherein said means applies a second portion of second de-interleaving pattern as data is read from the single memory buffer in order to improve the de-interleaving system.

10. In the claims 3, 17, Shiu discloses memory buffer stores the data, and wherein said means performs first and second de-interleaving as the stored data is read from single memory buffer (See figure 5, col. 13, lines 58-60).

11. In the claim 4, Shiu et al. discloses the limitations of claim 1 above.

However, Shiu et al. is silent to disclosing the data comprises radio frames, memory buffer comprises a plurality of radio frame blocks, and means causes radio frames to be stored in radio frame blocks

Delvaux et al. discloses the data comprises radio frames, memory buffer comprises a plurality of radio frame blocks, and means causes radio frames to be stored in radio frame blocks (See figure 11A, 11B, col. 21, lines 13-17).

Both Shiu and Delvaux discloses de-interleaving radio frames. Delvaux et al. recognizes the data comprises radio frames, memory buffer comprises a plurality of radio frame blocks, and means causes radio frames to be stored in radio frame blocks. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the system of Shiu with the teaching of Delvaux to apply a first

portion of a second de-interleaving pattern as data is written to the single memory buffer , and wherein said means applies a second portion of second de-interleaving pattern as data is read from the single memory buffer in order to improve the de-interleaving system.

12. In the claim 5, Shiu et al. discloses the data is transmitted over one or more physical channels, wherein each of radio frames comprises a physical channel frame associated with each physical channel, each of radio frame blocks comprises a physical channel block associated with each physical channel, and means causes said physical channel frames to be stored in said physical channel blocks (see col. 8, lines 34-44, col. 9, lines 47-67).

13. In the claims 12, 14, Shiu et al. reassembling one or more physical channels from the data stored in memory buffer (see col. 8, lines 34-44, col. 9, lines 47-67); perform a second removal of discontinuous transmission indication bits from the data stored in memory buffer (see col. 9, lines 23-67); demultiplexing (see col. 10, lines 58-60) the data stored in memory buffer into a plurality of transport channel (see col. 5, line 24); and reassembling transport blocks from data stored in memory buffer wherein the data comprises radio frames (see col. 8, lines 34-44, col. 9, lines 47-67).

However, Shiu et al. is silent to disclosing perform a second removal of discontinuous transmission indication bits from the data stored in memory buffer.

Delvaux discloses perform a second removal of discontinuous transmission indication bits from the data stored in memory buffer (see figures 11A, 11B, see col. 21, lines 14-16).

Both Shiu and Delvaux discloses de-interleaving radio frames. Delvaux et al. recognizes perform a second removal of discontinuous transmission indication bits from the data stored in memory buffer (see figures 11A, 11B, see col. 21, lines 14-16). Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the system of Shiu with the teaching of Delvaux to perform perform a second removal of discontinuous transmission indication bits from the data stored in memory buffer in order to improve the de-interleaving system.

14. In the claim 18, Shiu discloses the memory buffer is divided into at least nine logical partitions represents at least nine radio frame blocks (see col. 7, lines 1-6, memory banks).

15. In the claim 19, Delvaux discloses wherein said means can de-interleave data from eight radio frames while a ninth radio frame is being received (see figures 11A, 11B, col. 21, lines 12-17).

16. In the claim 20, Shiu discloses the physical channel blocks are sized to accommodate a maximum physical channel frame size allowed by the system (see col. 7, lines 40-45).

17. In the claims 20, 21, Shiu discloses wherein the radio frame blocks are sized to handle a maximum frame sized allowed by the system (see col. 14, lines 58-62).

18. In the claim 22, Shiu discloses wherein the radio frame blocks are sized to handle a maximum frame size allowed by the system (see col. 14, lines 58-62).

19. In the claim 23, Delvaux et al. discloses wherein said reading further effectively performs reassembling physical channels and reassembling radio frames (see col. 11, line 24, col. 12, line 48, reassembled).

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to CHUONG T. HO whose telephone number is (571) 272-3133. The examiner can normally be reached on 8:00 am to 4:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Huy Vu can be reached on (571) 272-3155. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

09/08/06

HUY D. VU
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600